k) saving the resulting vectors as vector set V_N and saving the list of undetected faults as list G_{N-1};

l) repeating step g) to i) M+1 times with N having values M to 0;

These and other aspects of the invention will become apparent from the following description, when taken in combination with the accompanying drawings, in which :

Figs. 1(a-b) are depictions
~~Fig. 1 is a depiction~~ of a test vector;
Figs. 2(a-c) are flow charts
~~Fig. 2 is a flow chart~~ of the steps involved in the method of re-ordering test vectors for maximising the fault coverage on a digital circuit;

Fig. 3 is a legend to terms used in the flow chart of Fig. 1, and

Fig. 4 is an example of a graph of fault coverage showing the number of faults detected against the number of vectors for the original vectors and vectors after using the new method/algorithm.

Reference is first made to Figs. 2 and 3 of the drawings which depict a flow chart of a sequence of steps involved in re-ordering test vectors to provide a test vector generation pattern for maximising the fault coverage on an integrated digital circuit using a limited number of test vectors.

In stage 1, (steps a) to f) an initial set of vectors are provided (step a) and these are copied to form a set of test vectors T_0 to place these vectors in a near-optimal order for detecting a set of faults F_0. Stage 1 has two principal steps. In the first step